



PRELIMINARY

NLT Technologies, Ltd.

TFT COLOR LCD MODULE

NL160120AC27-32

54 cm (21.3 Type)

UXGA

LVDS Interface (2 port)

PRELIMINARY DATA SHEET

DOD-PP-1268 (2nd edition)

**This PRELIMINARY DATA SHEET is updated
document from DOD-PP-1244(1).**

**All information is subject to change without
notice. Please confirm the sales representative
before starting to design your system.**

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INTRODUCTION

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The products are classified into three quality grades: "**Standard**", "**Special**", and "**Specific**" of the highest grade of a quality assurance program at the choice of a customer. Each quality grade is designed for applications described below. Any customer who intends to use a product for application other than that of Standard quality grade is required to contact an NLT sales representative in advance.

The **Standard** quality grade applies to the products developed, designed and manufactured in accordance with the NLT standard quality assurance program, which are designed for such application as any failure or malfunction of the products (sets) or parts/components incorporated therein a customer uses are, directly or indirectly, free of any damage to death, human bodily injury or other property, like general electronic devices.

Examples: Computers, office automation equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment, industrial robots, etc.

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Examples: Military systems, aircraft control equipment, aerospace equipment, nuclear reactor control systems, medical equipment/devices/systems for life support, etc.

The quality grade of this product is the "**Standard**" unless otherwise specified in this document.



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1. OUTLINE

1.1 STRUCTURE AND PRINCIPLE

Color LCD module NL160120AC27-32 is composed of the amorphous silicon thin film transistor liquid crystal display (a-Si TFT LCD) panel structure with driver LSIs for driving the TFT (Thin Film Transistor) array and a backlight.

The a-Si TFT LCD panel structure is injected liquid crystal material into a narrow gap between the TFT array glass substrate and a color-filter glass substrate.

Grayscale data signals from a host system (e.g. signal generator, etc.) are modulated into best form for active matrix system by a signal processing board, and sent to the driver LSIs which drive the individual TFT arrays.

The TFT array as an electro-optical switch regulates the amount of transmitted light from the backlight assembly, when it is controlled by data signals. Color images are created by regulating the amount of transmitted light through the TFT array of red, green and blue dots.

1.2 APPLICATION

- Color monitor system

1.3 FEATURES

- Ultra-wide viewing angle (Ultra-Advanced Super Fine TFT (UA-SFT))
- High luminance
- High contrast
- High resolution
- Low reflection
- Wide color gamut
- 256 gray scale in each R, G, B sub-pixel (8-bit), 16,777,216 colors
- LVDS interface
- Selectable LVDS data input map
- Small foot print
- Long life LED backlight type with an LED driver board



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2. GENERAL SPECIFICATIONS

<i>Display area</i>	432.0 (H) × 324.0 (V) mm
<i>Diagonal size of display</i>	54 cm (21.3 inches)
<i>Drive system</i>	a-Si TFT active matrix
<i>Display color</i>	16,777,216 colors
<i>Pixel</i>	1,600 (H) × 1,200 (V) pixels (1 pixel consists of 3 sub-pixels (RGB).)
<i>Pixel arrangement</i>	RGB (Red dot, Green dot, Blue dot) vertical stripe
<i>Dot pitch</i>	0.090 (H) × 0.270 (V) mm
<i>Pixel pitch</i>	0.270 (H) × 0.270 (V) mm
<i>Module size</i>	457.0 (W) × 350.0 (H) × 21.5 (D) mm (typ.)
<i>Weight</i>	(2,700) g (typ.)
<i>Contrast ratio</i>	1400:1 (typ.)
<i>Viewing angle</i>	At the contrast ratio ≥ 10:1 • Horizontal: Right side 88° (typ.), Left side 88° (typ.) • Vertical: Up side 88° (typ.), Down side 88° (typ.)
<i>Designed viewing direction</i>	Viewing angle with optimum grayscale ($\gamma \approx$ DICOM): normal axis (perpendicular) Note1
<i>Polarizer surface</i>	Antiglare
<i>Polarizer pencil-hardness</i>	2H (min.) [by JIS K5600]
<i>Color gamut</i>	At LCD panel center (72) % (typ.) [against NTSC color space]
<i>Response time</i>	$T_{on} + T_{off}$ (10% ← → 90%) (40) ms (typ.)
<i>Luminance</i>	At the maximum luminance 900 cd/m ² (typ.)
<i>Signal system</i>	2 ports LVDS interface (THC63LVD824A THine Electronics, Inc. or equivalent) [RGB 8-bit signals, Data enable signal (DE), Dot clock (CK)]
<i>Power supply voltage</i>	LCD panel signal processing board: 12.0V LED driver board: 12.0V
<i>Backlight</i>	LED backlight type with LED driver board
<i>Power consumption</i>	At checkered flag pattern, the maximum luminance (57) W (typ.)

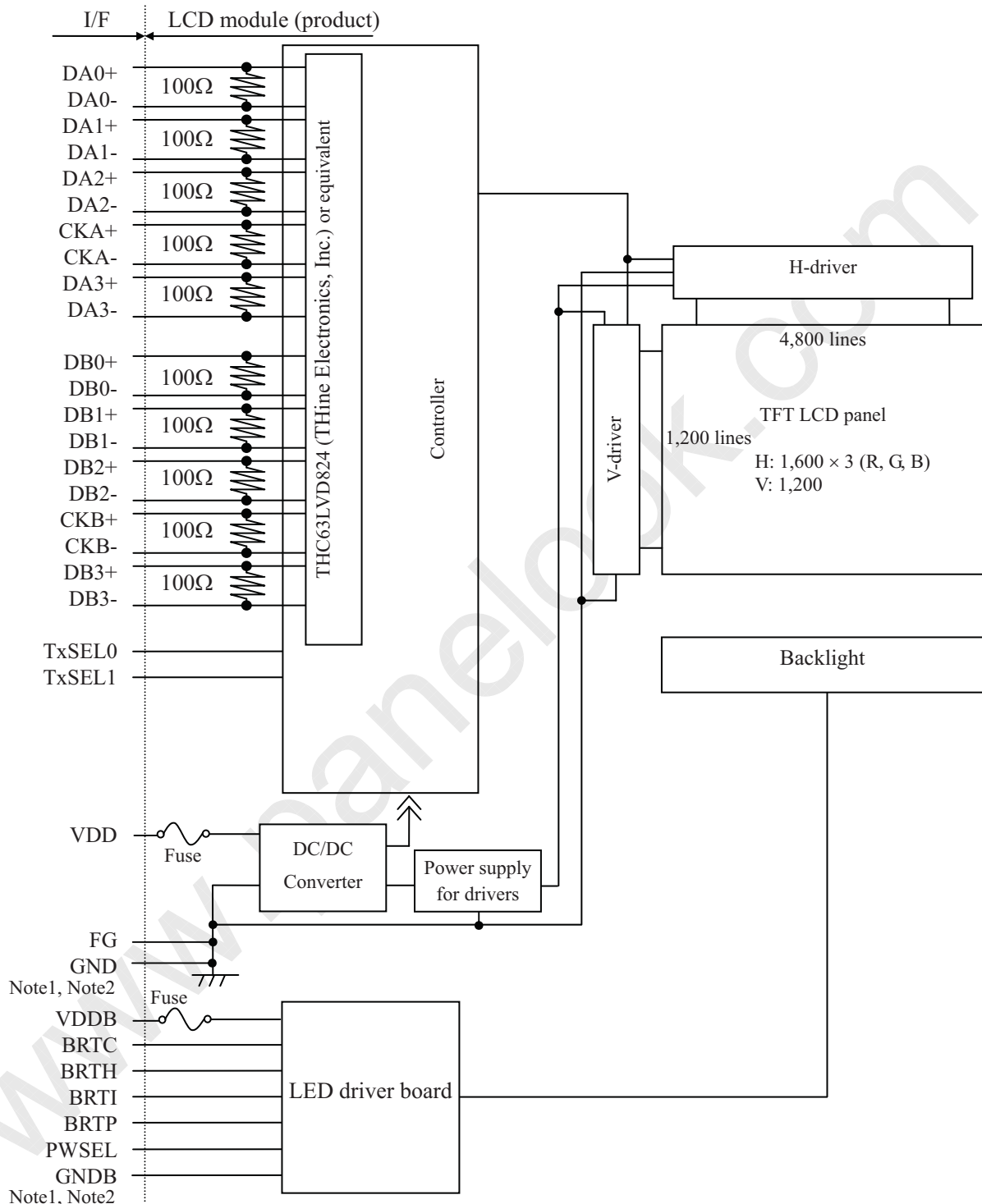
Note1: When the product luminance is 450cd/m², the gamma characteristic is designed to $\gamma \approx$ DICOM.

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3. BLOCK DIAGRAM



Note1: Relations between GND (Signal ground), FG (Frame ground) and GNDB (LED driver board ground) in the LCD module are as follows.

GND - FG	Connected
GND - GNDB	Not connected
FG - GNDB	Not connected

Note2: GND, FG and GNDB must be connected to customer equipment's ground, and it is recommended that these grounds be connected together in customer equipment.



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4. DETAILED SPECIFICATIONS

4.1 MECHANICAL SPECIFICATIONS

Parameter	Specification	Unit
Module size	457.0 ±0.5 (W) × 350.0 ±0.5 (H) × 21.5 (typ., D) 23.0 (max. D) Note1, Note2	mm
Display area	432.0 (H) × 324.0 (V) Note2	mm
Weight	(2,700) (typ.), (2,980) (max.)	g

Note1: Excluding warpage of the cover for LED driver board.

Note2: See "8. OUTLINE DRAWINGS".

4.2 ABSOLUTE MAXIMUM RATINGS

Parameter			Symbol	Rating	Unit	Remarks
Power supply voltage	LCD panel signal processing board		VDD	-0.3 to +14.0	V	Ta = 25℃
	LED driver board		VDDDB	-0.3 to +15.0	V	
Input voltage for signals	LCD panel signal processing board Note1		Vi	-0.3 to +3.45	V	VDD= 12.0V
	LED driver board	BRTI signal	VBI	-0.3 to +1.5	V	VDDDB= 12.0V
		BRTP signal	VBP	-0.3 to +5.5	V	
		BRTC signal	VBC	-0.3 to +5.5	V	
		PWSEL signal	VBS	-0.3 to +5.5	V	
Storage temperature			Tst	-20 to +60	℃	-
Operating temperature	Front surface		TopF	(0 to +60)	℃	Note2
	Rear surface		TopR	(0 to +60)	℃	Note3
Relative humidity Note4			RH	≤ 95	%	Ta ≤ 40℃
				≤ 85	%	40℃ < Ta ≤ 50℃
				≤ 70	%	50℃ < Ta ≤ 55℃
Absolute humidity Note4			AH	≤ 73 Note5	g/m ³	Ta > 55℃
Operating altitude			-	≤ 4,850	m	0℃ ≤ Ta ≤ 55℃
Storage altitude			-	≤ 13,600	m	-20℃ ≤ Ta ≤ 60℃

Note1: DA0+/-, DA1+/-, DA2+/-, DA3+/-, CKA+/-, DB0+/-, DB1+/-, DB2+/-, DB3+/-, CKB+/-

Note2: Measured at LCD panel surface (including self-heat)

Note3: Measured at LCD module's rear shield surface (including self-heat)

Note4: No condensation

Note5: Water amount at Ta = 55°C and RH = 70%



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4.3 ELECTRICAL CHARACTERISTICS

4.3.1 LCD panel signal processing board

(Ta = 25°C)

Parameter		Symbol	min.	typ.	max.	Unit	Remarks
Power supply voltage		VDD	10.8	12.0	13.2	V	-
Power supply current		IDD	-	(500) Note1	(700) Note2	mA	at VDD= 12.0V
Permissible ripple voltage		VRP	-	-	100	mVp-p	for VDD
Differential input threshold voltage	High	VTH	-	-	+100	mV	at VCM= 1.2V Note3, Note4
	Low	VTL	-100	-	-	mV	
Input voltage swing		VI	0	-	2.4	V	Note4
Terminating resistance		RT	-	100	-	Ω	-

Note1: Checkered flag pattern (by EIAJ ED-2522)

Note2: Pattern for maximum current

Note3: Common mode voltage for LVDS driver

Note4: DA0+/-, DA1+/-, DA2+/-, DA3+/-, CKA+/-, DB0+/-, DB1+/-, DB2+/-, DB3+/-, CKB+/-

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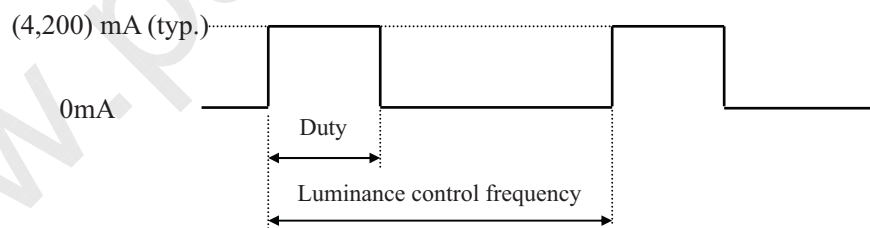
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4.3.2 LED Driver board

(Ta = 25°C)

Parameter		Symbol	min.	typ.	max.	Unit	Remarks
Power supply voltage		VDDB	(11.4)	12.0	(12.6)	V	-
Power supply current		IDDB	-	(4,200)	TBD	mA	VDDB= 12.0V, At the maximum luminance control
Input voltage for signals	BRTI signal		VBI	0	-	1.0	V
	BRTP signal	High	VBPH	2.0	-	5.25	V
		Low	VBPL	0	-	0.8	V
	BRTC signal	High	VBCH	2.0	-	5.25	V
		Low	VBCL	0	-	0.8	V
	PWSEL signal	High	VBSH	2.0	-	5.25	V
		Low	VBSL	0	-	0.8	V
							-
Input current for signals	BRTI signal		IBI	TBD	-	TBD	μA
	BRTP signal	High	IBPH	-	-	TBD	μA
		Low	IBPL	TBD	-	-	μA
	BRTC signal	High	IBCH	-	-	TBD	μA
		Low	IBCL	TBD	-	-	μA
	PWSEL signal	High	IPSH	-	-	TBD	μA
		Low	IPSL	TBD	-	-	μA
							-

4.3.3 LED driver board current wave



At the maximum luminance control: 100%

At the minimum luminance control: (1)% (At frequency: 325 Hz)

Luminance control frequency: (255)Hz (typ.)

Note1: Luminance control frequency indicate the input pulse frequency, when select the external pulse control. See "4.6.2 Detail of BRTP timing".

Note2: The power supply lines (VDDB and GNDB) have large ripple voltage during luminance control. There is the possibility that the ripple voltage produces acoustic noise and signal wave noise in audio circuit and so on. Put a capacitor (5,000 to 6,000μF) between the power supply lines (VDDB and GNDB) to reduce the noise, if the noise occurred in the circuit..

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4.3.4 Power supply voltage ripple

2

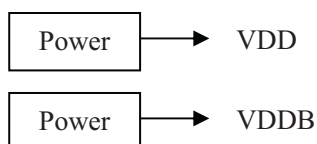
This product works, even if the ripple voltage levels are beyond the permissible values as following the table, but there might be noise on the display image.

Power supply voltage		Ripple voltage (Measure at input terminal of power supply)	Unit
VDD	12.0V	≤ 100	mVp-p
VDDDB	12.0V	≤ 200	mVp-p

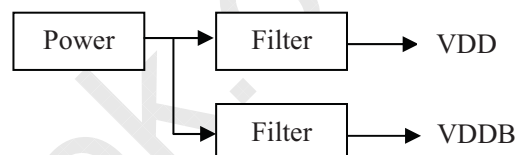
Note1: The permissible ripple voltage includes spike noise.

Example of the power supply connection

a) Separate the power supply



b) Put in the filter



4.3.5 Fuse

2

Parameter	Fuse		Rating	Fusing current	Remarks
	Type	Supplier			
VDD	FCC16132AB	KAMAYA ELECTRIC Co., Ltd.	1.25A	2.5A, 5 seconds maximum	Note1
			32V		
VDDB	CCF1N10	KOA Corporation	10A	20 A, 1 seconds maximum	
			60 V		

Note1: The power supply capacity should be more than the fusing current. If it is less than the fusing current, the fuse may not blow in a short time, and then nasty smell, smoke and so on may occur.

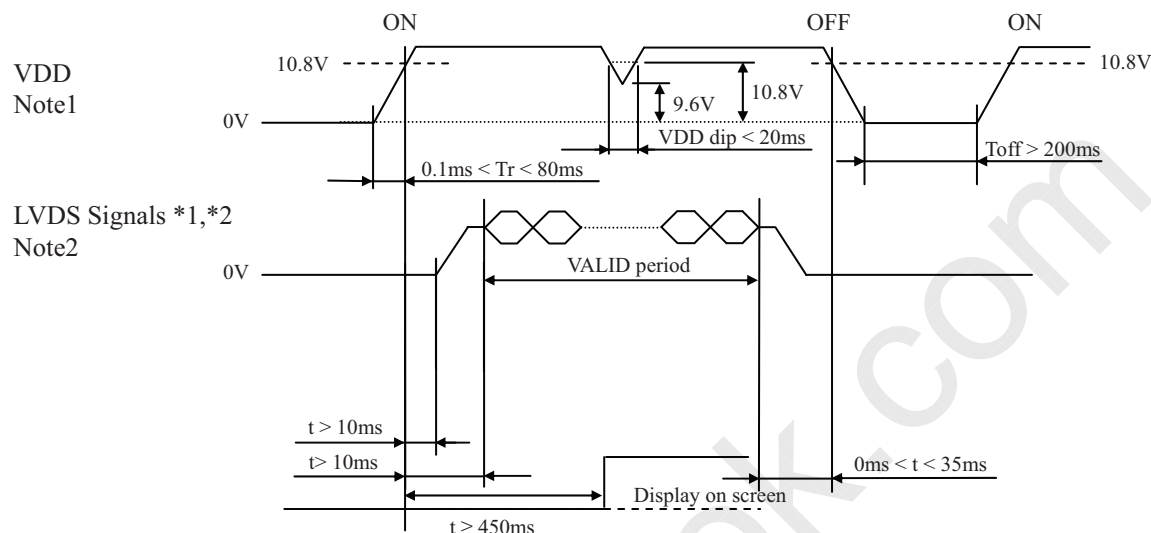
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4.4 POWER SUPPLY VOLTAGE SEQUENCE

4.4.1 LCD panel signal processing board



*1: DA0+/-, DA1+/-, DA2+/-, DA3+/-, CKA+/-, DB0+/-, DB1+/-, DB2+/-, DB3+/- and CKB+/-

*2: LVDS signals should be measured at the terminal of 100Ω resistance.

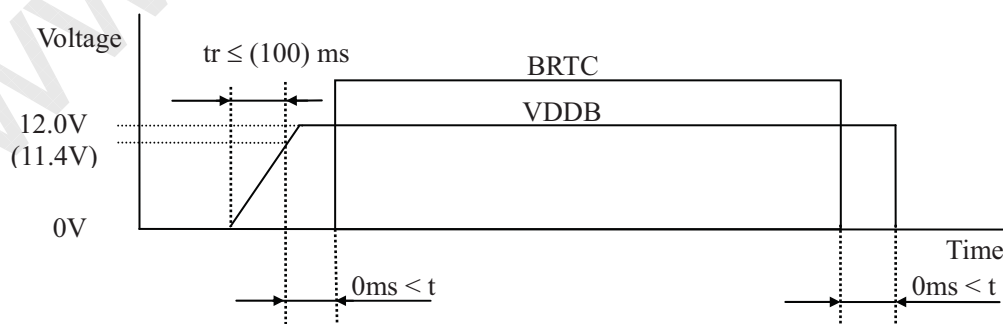
Note1: If there is a voltage variation (voltage drop) at the rising edge of VCC below 10.8V, there is a possibility that a product does not work due to a protection circuit.

Note2: LVDS signals must be set to Low or High-impedance, except the VALID period (See above sequence diagram), in order to avoid the circuitry damage.

If some of signals are cut while this product is working, even if the signal input to it once again, it might not work normally. If a customer stops the display and function signals, VCC also must be shut down.

Note3: The backlight should be turned on within the valid period of LVDS signals, in order to avoid unstable data display.

4.4.2 LED driver board



Note1: The backlight should be turned on within the valid period of LVDS signals, in order to avoid unstable data display.

Note2: If t_r is more than (100)ms, the backlight will be turned off by a protection circuit for LED driver board.

Note3: When VDDB is 0V or BRTC is Low, PWSEL must be set to Low or Open.

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4.5 CONNECTIONS AND FUNCTIONS FOR INTERFACE PINS

4.5.1 LCD panel signal processing board

CN1 Socket (LCD module side): DF19G-30P-1H (56) (Hirose Electric Co., Ltd. (HRS))

Adaptable plug: DF19-30S-1C (Hirose Electric Co., Ltd. (HRS))

Pin No.	Symbol	Signal	Remarks																		
1	DA0-	Pixel data A0	Odd pixel data Input (LVDS differential signal)		Note1																
2	DA0+																				
3	DA1-	Pixel data A1	Odd pixel data Input (LVDS differential signal)		Note1																
4	DA1+																				
5	DA2-	Pixel data A2	Odd pixel data Input (LVDS differential signal)		Note1																
6	DA2+																				
7	GND	Ground	Signal ground		Note2																
8	CKA-	Pixel clock	Odd pixel clock Input (LVDS differential signal)		Note1																
9	CKA+																				
10	DA3-	Pixel data A3	Odd pixel data Input (LVDS differential signal)		Note1																
11	DA3+																				
12	DB0-	Pixel data B0	Even pixel data Input (LVDS differential signal)		Note1																
13	DB0+																				
14	GND	Ground	Signal ground		Note2																
15	DB1-	Pixel data B1	Even pixel data Input (LVDS differential signal)		Note1																
16	DB1+																				
17	GND	Ground	Signal ground		Note2																
18	DB2-	Pixel data B2	Even pixel data Input (LVDS differential signal)		Note1																
19	DB2+																				
20	CKB-	Pixel clock	Even pixel clock Input (LVDS differential signal)		Note1																
21	CKB+																				
22	DB3-	Pixel data B3	Even pixel data Input (LVDS differential signal)		Note1																
23	DB3+																				
24	GND	Ground	Signal ground		Note2																
25	TxSEL0	Selection of LVDS data input map	Note3, Note4	<table><tr><td>TxSEL1</td><td>TxSEL0</td><td>Mode</td></tr><tr><td>Open</td><td>Open</td><td>A</td></tr><tr><td>Open</td><td>Low</td><td>B</td></tr><tr><td>Low</td><td>Open</td><td>C</td></tr><tr><td>Low</td><td>Low</td><td>A</td></tr></table>			TxSEL1	TxSEL0	Mode	Open	Open	A	Open	Low	B	Low	Open	C	Low	Low	A
TxSEL1	TxSEL0			Mode																	
Open	Open			A																	
Open	Low			B																	
Low	Open			C																	
Low	Low	A																			
26	TxSEL1																				
27	GND	Power supply	12V																		
28	VDD																				
29	VDD																				
30	VDD																				

Note1: Twist pair wires with 100Ω (Characteristic impedance) should be used between LCD panel signal processing board and LVDS transmitter.

Note2: All GND and VDD terminals should be used without any non-connected lines.

Note3: This terminal is pulled-up in the product.

Note4: See "4.7 LVDS DATA INPUT MAP".

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4.5.2 LED driver board

CN201 socket (LCD module side): DF3Z-10P-2H (2*) (HIROSE ELECTRIC Co., Ltd.)

Adaptable plug: DF3-10S-2C (HIROSE ELECTRIC Co., Ltd.)

Pin No.	Symbol	Function	Description
1	GNDB	LED driver board ground	Note1
2	GNDB		
3	GNDB		
4	GNDB		
5	GNDB		
6	VDDB	Power supply	Note1
7	VDDB		
8	VDDB		
9	VDDB		
10	VDDB		

Note1: All VDDB and GNDB terminals should be used without any non-connected lines.

CN202 socket (LCD module side): IL-Z-9PL-SMTYE (Japan Aviation Electronics Industry Limited (JAE))

Adaptable plug: IL-Z-9S-S125C3 (Japan Aviation Electronics Industry Limited (JAE))

Pin No.	Symbol	Function	Description
1	GNDB	LED driver board ground	Note1
2	GNDB		
3	N.C.	-	Keep this pin Open.
4	BRTC	Backlight ON/OFF control signal	High or Open: Backlight ON Low: Backlight OFF
5	BRTH	Luminance control terminal	Note2
6	BRTI		
7	BRTP	BRTP signal	
8	GNDB	LED driver board ground	Note1
9	PWSEL	Selection of luminance control signal method	Note2, Note3

Note1: All GNDB terminals should be used without any non-connected lines.

Note2: See "4.6.1 LUMINANCE CONTROL".

Note3: When VDDB is 0V or BRTC is Low, PWSEL must be set to Low or Open.

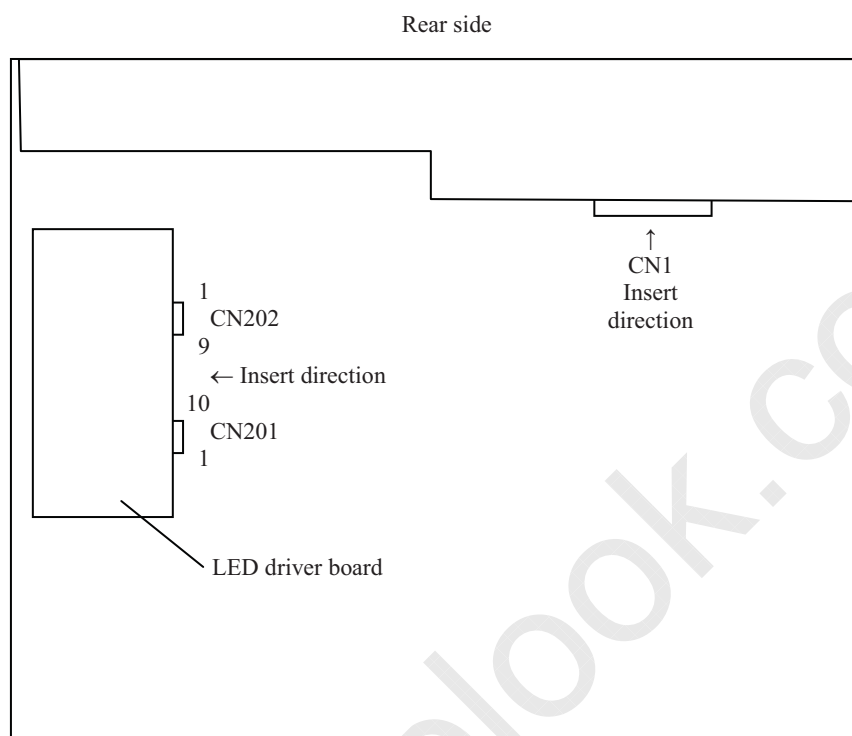


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4.5.3 Positions of socket



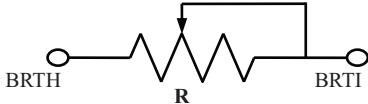
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4.6 LUMINANCE CONTROL

4.6.1 Luminance control methods

Method	Adjustment and luminance ratio	PWSEL terminal	BRTP terminal						
Variable resistor control Note1	• Adjustment The variable resistor (R) for luminance control should be 10kΩ ±5%, 1/10W. Minimum point of the resistance is the minimum luminance and maximum point of the resistance is the maximum luminance. The resistor (R) must be connected between BRTH-BRTI terminals.  • Luminance ratio Note3 <table><tr><th>Resistance</th><th>Luminance ratio</th></tr><tr><td>0Ω</td><td>0%(Min. Luminance)</td></tr><tr><td>10 kΩ</td><td>100% (Max. Luminance)</td></tr></table>	Resistance	Luminance ratio	0Ω	0%(Min. Luminance)	10 kΩ	100% (Max. Luminance)	High or Open	Open
Resistance	Luminance ratio								
0Ω	0%(Min. Luminance)								
10 kΩ	100% (Max. Luminance)								
Voltage control Note1	• Adjustment Voltage control method works, when BRTH terminal is 0V and VBI voltage is input between BRTI-BRTH terminals. This control method can carry out continuation adjustment of luminance. Luminance is the maximum when BRTI terminal is Open. • Luminance ratio Note3 <table><tr><th>BRTI Voltage (VBI)</th><th>Luminance ratio</th></tr><tr><td>0V</td><td>0% (Min. Luminance)</td></tr><tr><td>1.0V</td><td>100% (Max. Luminance)</td></tr></table>	BRTI Voltage (VBI)	Luminance ratio	0V	0% (Min. Luminance)	1.0V	100% (Max. Luminance)		
BRTI Voltage (VBI)	Luminance ratio								
0V	0% (Min. Luminance)								
1.0V	100% (Max. Luminance)								
Pulse width modulation Note1 Note2 Note4	• Adjustment Pulse width modulation (PWM) method works, when PWSEL terminal is Low and PWM signal (BRTP signal) is input into BRTP terminal. The luminance is controlled by duty ratio of BRTP signal. • Luminance ratio Note3 <table><tr><th>Duty ratio</th><th>Luminance ratio</th></tr><tr><td>(0.01)</td><td>(1)% (Min. Luminance) (At frequency: 325 Hz)</td></tr><tr><td>1.0</td><td>100% (Max. Luminance)</td></tr></table>	Duty ratio	Luminance ratio	(0.01)	(1)% (Min. Luminance) (At frequency: 325 Hz)	1.0	100% (Max. Luminance)	Low	BRTP signal
Duty ratio	Luminance ratio								
(0.01)	(1)% (Min. Luminance) (At frequency: 325 Hz)								
1.0	100% (Max. Luminance)								

Note1: In case of the variable resistor control method and the voltage control method, noises may appear on the display image depending on the input signals timing for LCD panel signal processing board.

Use PWM method, if interference noises appear on the display image!

Note2: The LED driver board will stop working, if the Low period of BRTP signal is more than 50ms while BRTP signal is High or Open. Then the backlight will not turn on anymore, even if BRTP signal is input again. This is not out of order. The LED driver board will start to work when power is supplied again.

Note3: These data are the target values.

Note4: See "4.6.2 Detail of BRTP timing".

PRELIMINARY

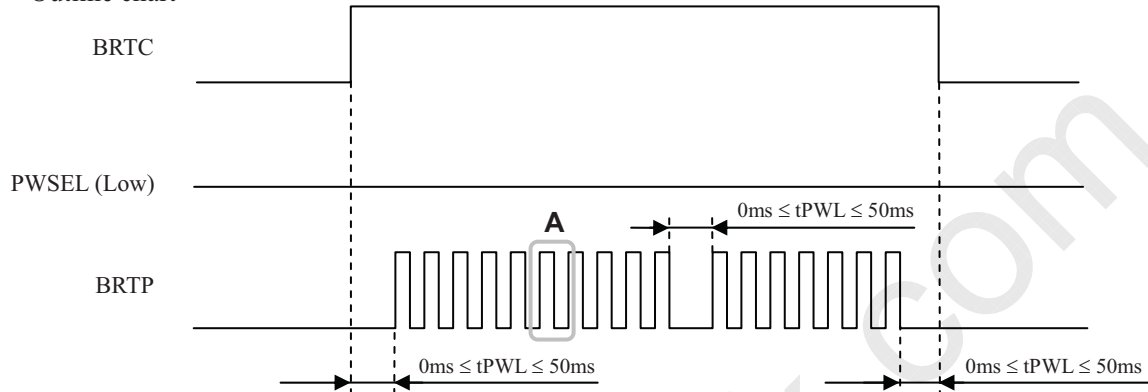
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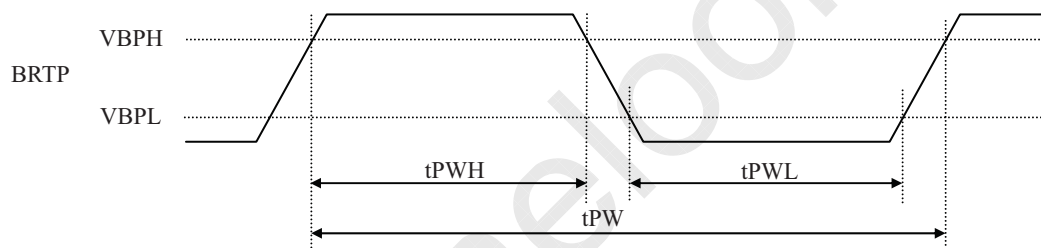
4.6.2 Detail of BRTP timing

(1) Timing diagrams

• Outline chart



• Detail of A part



(2) Each parameter

Parameter	Symbol	min.	typ.	max.	Unit	Remarks
Luminance control frequency	FL	(185)	-	(1,000)	Hz	Note1, Note2
External PWM pulse width	tPWH	(30)	-	-	μs	Note1, Note3

Note1: Definition of parameters is as follows.

$$FL = \frac{1}{tPW} \quad DL = \frac{tPWH}{tPW}$$

Note2: See the following formula for luminance control frequency.

$$\text{Luminance control frequency} = 1/tv \times (n+0.25) \text{ [or } (n+0.75)]$$

$$n = 1, 2, 3 \dots \dots$$

tv: Vertical cycle (See "4.9.1 Timing characteristics".)

The interference noise of luminance control frequency and input signal frequency for LCD panel signal processing board may appear on a display. Set up luminance control frequency so that the interference noise does not appear!

Note3: See "4.6.1 Luminance control methods".

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4.7 LVDS DATA INPUT MAP

4.7.1 Mode A

Input data		Transmitter		CN1	
		Pin	THC63LVDM83D	Pin	THC63LVD823B
Odd pixel data and control signal	RA2 →	51	TA0	53	R12
	RA3 →	52	TA1	54	R13
	RA4 →	54	TA2	57	R14
	RA5 →	55	TA3	58	R15
	RA6 →	56	TA4	59	R16
	RA7 →	3	TA5	60	R17
	GA2 →	4	TA6	63	G12
	GA3 →	6	TB0	64	G13
	GA4 →	7	TB1	65	G14
	GA5 →	11	TB2	66	G15
	GA6 →	12	TB3	67	G16
	GA7 →	14	TB4	68	G17
	BA2 →	15	TB5	73	B12
	BA3 →	19	TB6	74	B13
	BA4 →	20	TC0	75	B14
	BA5 →	22	TC1	76	B15
	BA6 →	23	TC2	77	B16
	BA7 →	24	TC3	78	B17
	Note3 RSVD →	27	TC4	7	RSVD
	Note3 RSVD →	28	TC5	8	RSVD
	DE →	30	TC6	9	DE
	RA0 →	50	TD0	51	R10
	RA1 →	2	TD1	52	R11
	GA0 →	8	TD2	61	G10
	GA1 →	10	TD3	62	G11
	BA0 →	16	TD4	69	B10
	BA1 →	18	TD5	70	B11
	Note3 RSVD →	25	TD6	-	
	CLK →	31	CLKIN	10	CLK
Even pixel data	RB2 →	51	TA0	81	R22
	RB3 →	52	TA1	82	R23
	RB4 →	54	TA2	83	R24
	RB5 →	55	TA3	84	R25
	RB6 →	56	TA4	85	R26
	RB7 →	3	TA5	86	R27
	GB2 →	4	TA6	91	G22
	GB3 →	6	TB0	92	G23
	GB4 →	7	TB1	93	G24
	GB5 →	11	TB2	94	G25
	GB6 →	12	TB3	95	G26
	GB7 →	14	TB4	96	G27
	BB2 →	15	TB5	99	B22
	BB3 →	19	TB6	100	B23
	BB4 →	20	TC0	1	B24
	BB5 →	22	TC1	2	B25
	BB6 →	23	TC2	5	B26
	BB7 →	24	TC3	6	B27
	Note3 RSVD →	27	TC4	-	
	Note3 RSVD →	28	TC5	-	
	Note3 RSVD →	30	TC6	-	
	RB0 →	50	TD0	79	R20
	RB1 →	2	TD1	80	R21
	GB0 →	8	TD2	89	G20
	GB1 →	10	TD3	90	G21
	BB0 →	16	TD4	97	B20
	BB1 →	18	TD5	98	B21
	Note3 RSVD →	25	TD6	-	
	CLK →	31	CLKIN	-	

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4.7.2 Mode B

Input data		Transmitter		CN1	
Note1		Pin	DS90CF383, C385	Pin	Symbol
Odd pixel data and control signal	RA7 →	51	TXIN0	Note2	1 DA0-
	RA6 →	52	TXIN1		2 DA0+
	RA5 →	54	TXIN2		
	RA4 →	55	TXIN3		
	RA3 →	56	TXIN4	TB1- →	3 DA1-
	RA2 →	3	TXIN6	TB1+ →	4 DA1+
	GA7 →	4	TXIN7		
	GA6 →	6	TXIN8	TC1- →	5 DA2-
	GA5 →	7	TXIN9	TC1+ →	6 DA2+
	GA4 →	11	TXIN12		7 GND
	GA3 →	12	TXIN13	TCLK1- →	8 CKA-
	GA2 →	14	TXIN14	TCLK1+ →	9 CKA+
	BA7 →	15	TXIN15		
	BA6 →	19	TXIN18	TD1- →	10 DA3-
	BA5 →	20	TXIN19	TD1+ →	11 DA3+
	BA4 →	22	TXIN20		
	BA3 →	23	TXIN21		
	BA2 →	24	TXIN22		
	Note3 RSVD →	27	TXIN24		
	Note3 RSVD →	28	TXIN25		
	DE →	30	TXIN26		
	RA1 →	50	TXIN27		
	RA0 →	2	TXIN5		
	GA1 →	8	TXIN10		
	GA0 →	10	TXIN11		
	BA1 →	16	TXIN16		
	BA0 →	18	TXIN17		
	Note3 RSVD →	25	TXIN23		
	CLK →	31	CLKIN		
Even pixel data	RB7 →	51	TXIN0		
	RB6 →	52	TXIN1	TA2- →	12 DB0-
	RB5 →	54	TXIN2	TA2+ →	13 DB0+
	RB4 →	55	TXIN3		14 GND
	RB3 →	56	TXIN4	TB2- →	15 DB1-
	RB2 →	3	TXIN6	TB2+ →	16 DB1+
	GB7 →	4	TXIN7		17 GND
	GB6 →	6	TXIN8	TC2- →	18 DB2-
	GB5 →	7	TXIN9	TC2+ →	19 DB2+
	GB4 →	11	TXIN12		
	GB3 →	12	TXIN13	TCLK2- →	20 CKB-
	GB2 →	14	TXIN14	TCLK2+ →	21 CKB+
	BB7 →	15	TXIN15		
	BB6 →	19	TXIN18	TD2- →	22 DB3-
	BB5 →	20	TXIN19	TD2+ →	23 DB3+
	BB4 →	22	TXIN20		24 GND
	BB3 →	23	TXIN21		25 TxSEL0
	BB2 →	24	TXIN22		26 TxSEL1
	Note3 RSVD →	27	TXIN24		27 GND
	Note3 RSVD →	28	TXIN25		28 VDD
	Note3 RSVD →	30	TXIN26		29 VDD
	RB1 →	50	TXIN27		30 VDD
	RB0 →	2	TXIN5		
	GB1 →	8	TXIN10		
	GB0 →	10	TXIN11		
	BB1 →	16	TXIN16		
	BB0 →	18	TXIN17		
	Note3 RSVD →	25	TXIN23		
	CLK →	31	CLKIN		

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4.7.3 Mode C

Input data		Transmitter		CN1	
Note1		Pin	DS90CF383, C385	Pin	Symbol
Odd pixel data and control signal	RA0	→	51 TXIN0	Note2	1 DA0-
	RA1	→	52 TXIN1		2 DA0+
	RA2	→	54 TXIN2	TA1- →	3 DA1-
	RA3	→	55 TXIN3	TA1+ →	4 DA1+
	RA4	→	56 TXIN4	TB1- →	5 DA2-
	RA5	→	3 TXIN6	TB1+ →	6 DA2+
	GA0	→	4 TXIN7	TC1- →	7 GND
	GA1	→	6 TXIN8	TC1+ →	8 CKA-
	GA2	→	7 TXIN9	TCLK1- →	9 CKA+
	GA3	→	11 TXIN12	1st	10 DA3-
	GA4	→	12 TXIN13		11 DA3+
	GA5	→	14 TXIN14	TD1- →	
	BA0	→	15 TXIN15	TD1+ →	
	BA1	→	19 TXIN18		
	BA2	→	20 TXIN19		
	BA3	→	22 TXIN20		
	BA4	→	23 TXIN21		
	BA5	→	24 TXIN22		
	Note3 RSVD	→	27 TXIN24		
	Note3 RSVD	→	28 TXIN25		
	DE	→	30 TXIN26		
	RA6	→	50 TXIN27		
	RA7	→	2 TXIN5		
	GA6	→	8 TXIN10		
	GA7	→	10 TXIN11		
	BA6	→	16 TXIN16		
	BA7	→	18 TXIN17		
	Note3 RSVD	→	25 TXIN23		
	CLK	→	31 CLKIN		
Even pixel data	RB0	→	51 TXIN0	Note2	12 DB0-
	RB1	→	52 TXIN1		13 DB0+
	RB2	→	54 TXIN2	TA2- →	14 GND
	RB3	→	55 TXIN3	TA2+ →	15 DB1-
	RB4	→	56 TXIN4	TB2- →	16 DB1+
	RB5	→	3 TXIN6	TB2+ →	17 GND
	GB0	→	4 TXIN7	TC2- →	18 DB2-
	GB1	→	6 TXIN8	TC2+ →	19 DB2+
	GB2	→	7 TXIN9	TCLK2- →	20 CKB-
	GB3	→	11 TXIN12	TCLK2+ →	21 CKB+
	GB4	→	12 TXIN13	2nd	22 DB3-
	GB5	→	14 TXIN14		23 DB3+
	BB0	→	15 TXIN15	TD2- →	24 GND
	BB1	→	19 TXIN18	TD2+ →	25 TxSEL0
	BB2	→	20 TXIN19		26 TxSEL1
	BB3	→	22 TXIN20		27 GND
	BB4	→	23 TXIN21		28 VDD
	BB5	→	24 TXIN22		29 VDD
	Note3 RSVD	→	27 TXIN24		30 VDD
	Note3 RSVD	→	28 TXIN25		
	Note3 RSVD	→	30 TXIN26		
	RB6	→	50 TXIN27		
	RB7	→	2 TXIN5		
	GB6	→	8 TXIN10		
	GB7	→	10 TXIN11		
	BB6	→	16 TXIN16		
	BB7	→	18 TXIN17		
	Note3 RSVD	→	25 TXIN23		
	CLK	→	31 CLKIN		



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Note1: LSB (Least Significant Bit) – RA0, GA0, BA0, RB0, GB0, BB0

MSB (Most Significant Bit) – RA7, GA7, BA7, RB7, GB7, BB7

Note2: Twist pair wires with 100Ω (Characteristic impedance) should be used between LCD panel signal processing board and LVDS transmitter.

Note3: Input signal RSVD is not used inside the product, but do not keep pin open to avoid noise problem.

4.8 DISPLAY COLORS AND INPUT DATA SIGNALS

This product can display in equivalent to 16,777,216 colors in 256 gray scales in each RGB sub-pixel. Also the relation between display colors and input data signals is as the following table.

Display colors		Data signal (0: Low level, 1: High level)																							
		RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0	GA7	GA6	GA5	GA4	GA3	GA2	GA1	GA0	BA7	BA6	BA5	BA4	BA3	BA2	BA1	BA0
		RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	GB7	GB6	GB5	GB4	GB3	GB2	GB1	GB0	BB7	BB6	BB5	BB4	BB3	BB2	BB1	BB0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Red gray scale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	dark	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	↑					:							:							:					
	↓					:							:							:					
	bright	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Green gray scale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	↑					:							:							:					
	↓					:							:							:					
	bright	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0
Blue gray scale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
	↑					:							:							:					
	↓					:							:							:					
	bright	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1
Blue		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

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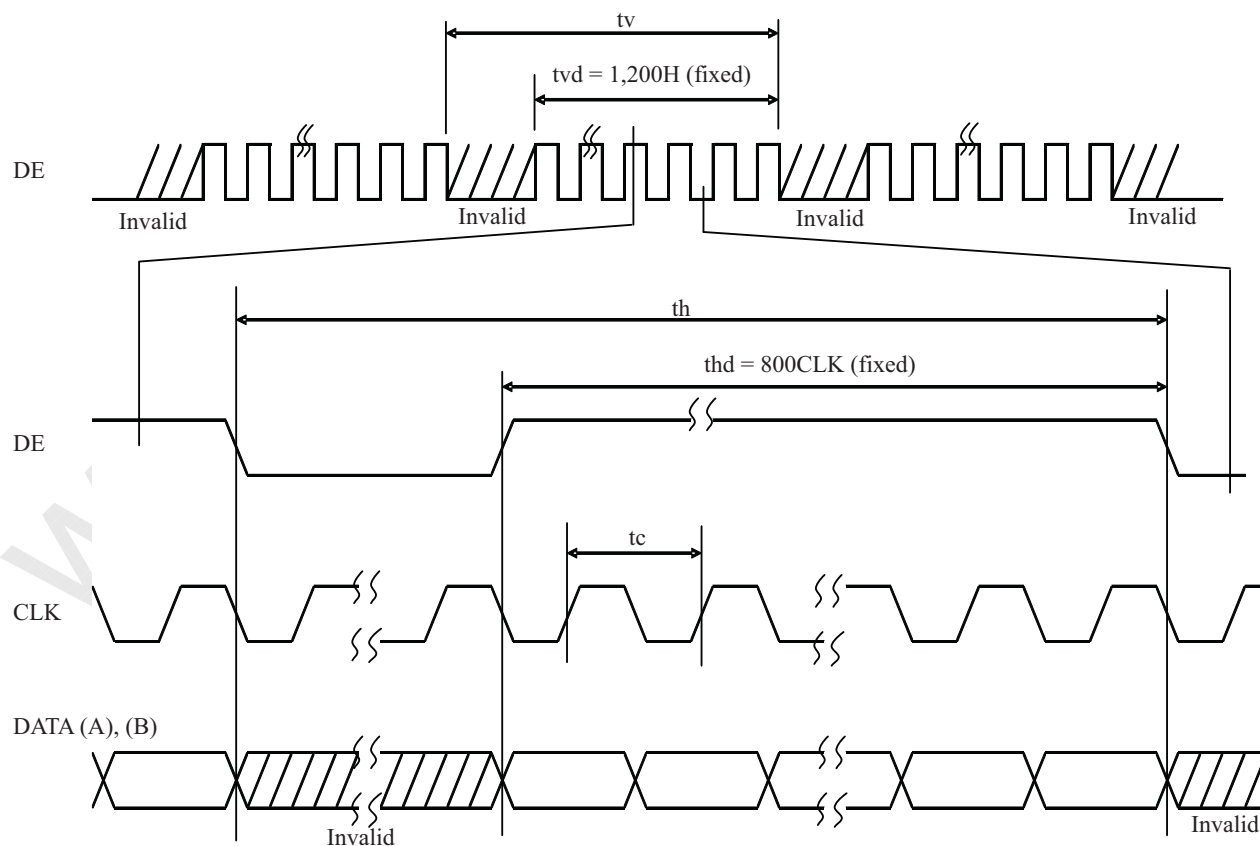
4.9 INPUT SIGNAL TIMINGS

4.9.1 Timing characteristics

	Parameter	Symbol	min.	typ.	max.	Unit	Remarks
CLK	Frequency	1/ tc	60.0	64.5	65.0	MHz	LVDS transmitter input
	Pulse width	tc	15.38	15.5	-	ns	
	Duty	-	See the data sheet of LVDS transmitter.			-	-
	Rise, fall	-				ns	
Horizontal	Cycle	th	13.1	13.3	19.2	μs	Note1
			848	860	1,156	CLK	
	Display period	thd	800			CLK	-
Vertical	Cycle	1/tv	59	60	61	Hz	-
		tv	1,206	1,250	-	H	
	Display period	tvd	1,200			H	-
DE, DATA	Setup time	-	See the data sheet of LVDS transmitter.			ns	-
	Hold time	-				ns	
	Rise, fall	-				ns	

Note1: During operation, fluctuation of horizontal cycle should be within ± 1 CLK.

4.9.2 Input signal timing chart

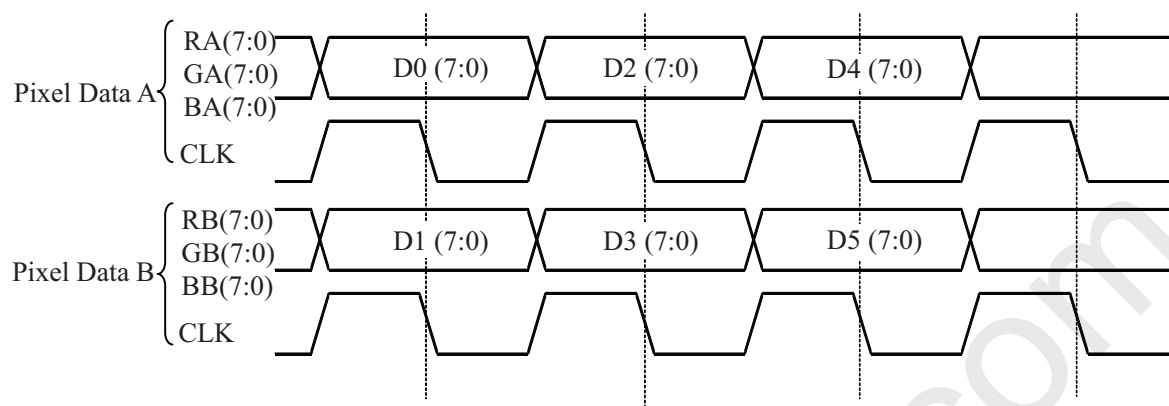


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4.10 LVDS DATA TRANSMISSION METHOD



4.11 DISPLAY POSITIONS

Odd pixel: RA= Red data
GA= Green data
BA= Blue data

Even pixel: RB= Red data
GB= Green data
BB= Blue data

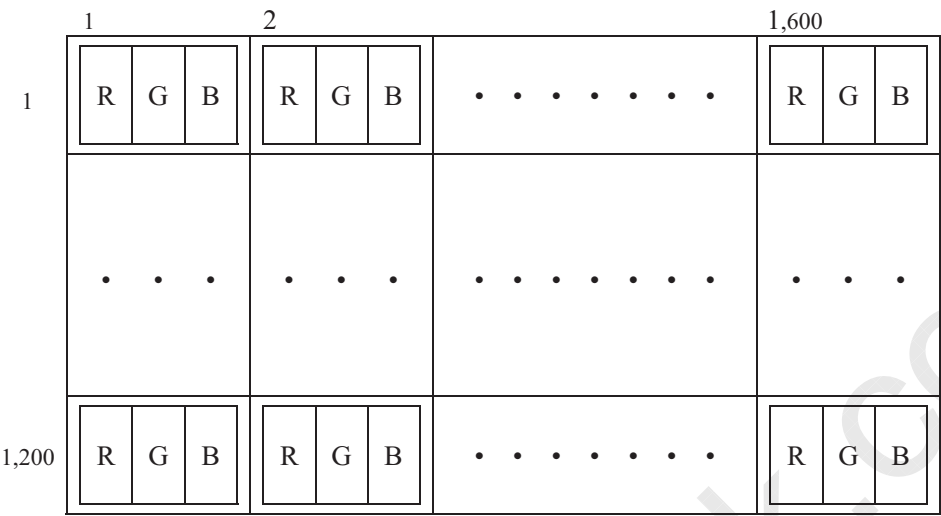
D (1, 1)			D (2, 1)		
RA	GA	BA	RB	GB	BB
↑					
D(1, 1)	D(2, 1)	...	D(X, 1)	...	D(1599, 1)
D(1, 2)	D(2, 2)	...	D(X, 2)	...	D(1599, 2)
⋮	⋮	⋮	⋮	⋮	⋮
D(1, Y)	D(2, Y)	...	D(X, Y)	...	D(1599, Y)
⋮	⋮	⋮	⋮	⋮	⋮
D(1, 1199)	D(2, 1199)	...	D(X, 1199)	...	D(1599, 1199)
D(1, 1200)	D(2, 1200)	...	D(X, 1200)	...	D(1599, 1200)

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4.12 PIXEL ARRANGNMENT



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4.13 OPTICS

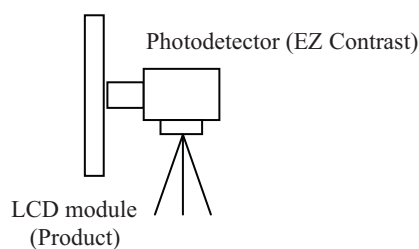
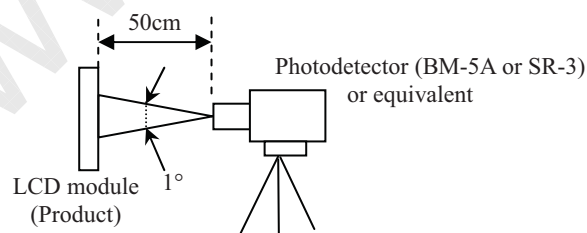
4.13.1 Optical characteristics

(Note1, Note2)

Parameter		Condition	Symbol	min.	typ.	max.	Unit	Measuring instrument	Remarks
Luminance		White at center $\theta R = 0^\circ, \theta L = 0^\circ, \theta U = 0^\circ, \theta D = 0^\circ$	L	TBD	900	-	cd/m ²	BM-5A or SR-3	Note3
Contrast ratio		White/Black at center $\theta R = 0^\circ, \theta L = 0^\circ, \theta U = 0^\circ, \theta D = 0^\circ$	CR	TBD	1,400	-	-	BM-5A or SR-3	Note3 Note5
Luminance uniformity		255/255 gray scale $\theta R = 0^\circ, \theta L = 0^\circ, \theta U = 0^\circ, \theta D = 0^\circ$	LU1023	(80)	-	-	%	BM-5A or SR-3	Note4 Note6
Chromaticity	White	x coordinate	Wx	(0.269)	0.299				Note3 Note8
		y coordinate	Wy	(0.285)	0.315	(0.345)	-		
	Red	x coordinate	Rx	-	(0.65)	-	-		
		y coordinate	Ry	-	(0.33)	-	-		
	Green	x coordinate	Gx	-	(0.29)	-	-		
		y coordinate	Gy	-	(0.60)	-	-		
	Blue	x coordinate	Bx	-	(0.15)	-	-		
		y coordinate	By	-	(0.07)	-	-		
Color uniformity		204/255 gray scale $\theta R = 0^\circ, \theta L = 0^\circ, \theta U = 0^\circ, \theta D = 0^\circ$	$\Delta u'v'$	-	-	0.01	-	SR-3	Note4 Note7
Color gamut		$\theta R = 0^\circ, \theta L = 0^\circ, \theta U = 0^\circ, \theta D = 0^\circ$ at center, against NTSC color space	C	(65)	(72)	-	%	SR-3	Note3
Response time		Black to White	Ton	-	(20)	(30)	ms	BM-5A	Note3 Note9
		White to Black	Toff	-	(20)	(30)	ms		
Viewing angle	Right	$\theta U = 0^\circ, \theta D = 0^\circ, CR \geq 10$	θR	70	88	-	°	BM-5A or EZ Contrast	Note3 Note10
	Left	$\theta U = 0^\circ, \theta D = 0^\circ, CR \geq 10$	θL	70	88	-	°		
	Up	$\theta R = 0^\circ, \theta L = 0^\circ, CR \geq 10$	θU	70	88	-	°		
	Down	$\theta R = 0^\circ, \theta L = 0^\circ, CR \geq 10$	θD	70	88	-	°		

Note1: These are initial characteristics.

Note2: Measurement conditions are as follows.

Ta = 25°C, VDD = 12.0V, VDDB = 12.0V, PWM: Duty 100%, Display mode: UXGA,
Horizontal cycle = 1/75.19 kHz, Vertical cycle = 1/60.0HzOptical characteristics are measured after 20 minutes from working the product, in the dark room.
Also measurement methods are as follows.

Note3: Product surface temperature at the maximum luminance control: TopF = 32°C

Note4: Product surface temperature at 450cd/m² luminance control: TopF = 30°CTemperature difference in display area: $\Delta TBD^\circ C$

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Note5: See "4.13.2 Definition of contrast ratio".

Note6: See "4.13.3 Definition of luminance uniformity".

Note7: See "4.13.4 Definition of color uniformity".

Note8: These coordinates are found on CIE 1931 chromaticity diagram.

Note9: See "4.13.5 Definition of response times".

Note10: See "4.13.6 Definition of viewing angles".

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4.13.2 Definition of contrast ratio

The contrast ratio is calculated by using the following formula.

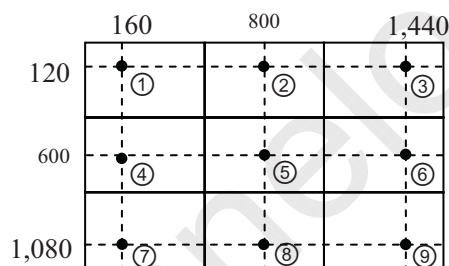
$$\text{Contrast ratio (CR)} = \frac{\text{Luminance of white screen}}{\text{Luminance of black screen}}$$

4.13.3 Definition of luminance uniformity

The luminance uniformity is calculated by using following formula.

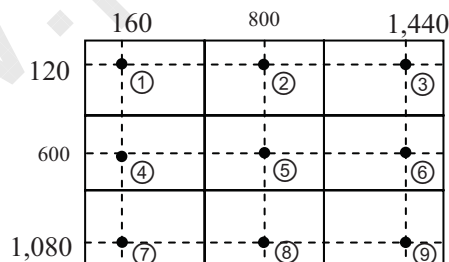
$$\text{Luminance uniformity (LU)} = \frac{\text{Minimum luminance from ① to ⑤}}{\text{Maximum luminance from ① to ⑤}}$$

The luminance is measured at near the 9 points shown below.



4.13.4 Definition of color uniformity

The color (u' , v') is measured at near the 9 points shown below.



The color uniformity in each measuring point is calculated by using the following formula.

$$\text{Color uniformity}(\Delta u'v') = \sqrt{(u'_x - u'_y)^2 + (v'_x - v'_y)^2}$$

u'_x, v'_x : u' , v' value at measuring point x.

u'_y, v'_y : u' , v' value at measuring point y.

2

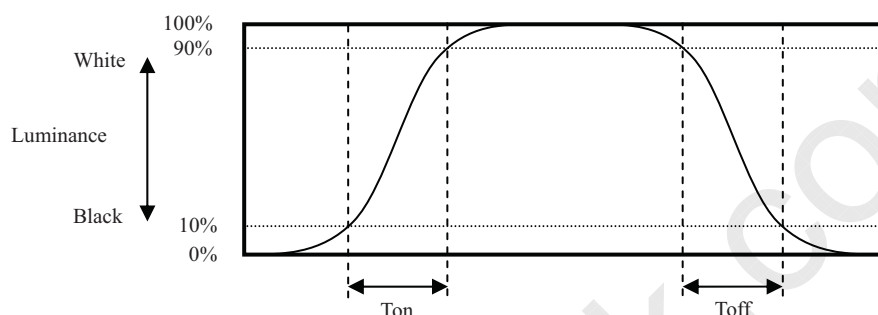
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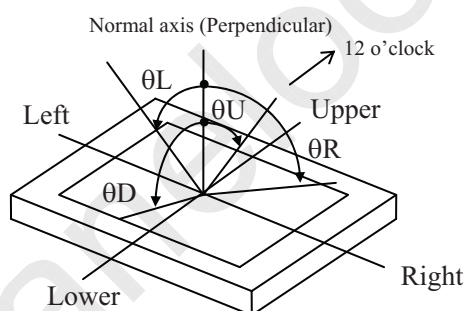
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4.13.5 Definition of response times

Response time is measured at the time when the luminance changes from "black" to "white", or "white" to "black" on the same screen point, by photo-detector. Ton is the time when the luminance changes from 10% up to 90%. Also Toff is the time when the luminance changes from 90% down to 10% (See the following diagram.).



4.13.6 Definition of viewing angles



5. ESTIMATED LUMINANCE LIFETIME

The luminance lifetime is the time from initial luminance to half-luminance.

This lifetime is the estimated value, and is not guarantee value.

Condition		Estimated luminance lifetime (Life time expectancy) Note1, Note2, Note3	Unit
LED elementary substance	25°C (Ambient temperature of the product) Continuous operation, PWM: Duty 100%	70,000	h
	60°C (Surface temperature at screen) Continuous operation, PWM: Duty 100%	TBD	

Note1: Life time expectancy is mean time to half-luminance.

Note2: Estimated luminance lifetime is not the value for an LCD module but the value for LED elementary substance.

Note3: By ambient temperature, the lifetime changes particularly. Especially, in case the product works under high temperature environment, the lifetime becomes short.

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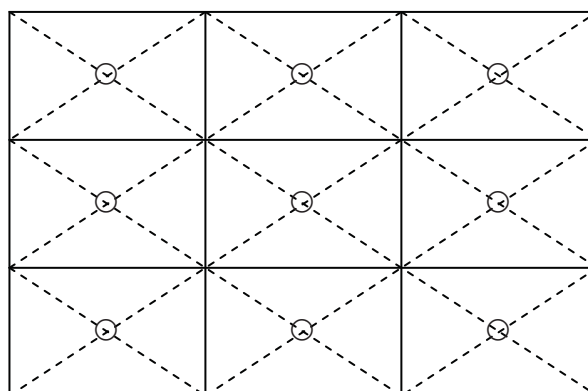
6. RELIABILITY TESTS

Test item		Condition	Judgment Note1
High temperature and humidity (Operation)		① $60 \pm 2^{\circ}\text{C}$, RH = 60%, 500hours ② Display data is white. Note2	No display malfunctions
Heat cycle (Operation)		① $0 \pm 3^{\circ}\text{C} \dots 1\text{hour}$ $60 \pm 3^{\circ}\text{C} \dots 1\text{hour}$ ② 50cycles, 4hours/cycle ③ Display data is white. Note2	
Thermal shock (Non operation)		① $-20 \pm 3^{\circ}\text{C} \dots 30\text{minutes}$ $60 \pm 3^{\circ}\text{C} \dots 30\text{minutes}$ ② 100cycles, 1hour/cycle ③ Temperature transition time is within 5 minutes.	
Vibration (Non operation)		① 5 to 100Hz, 11.76m/s^2 ② 1 minute/cycle ③ X, Y, Z directions ④ 10 times each directions	No display malfunctions No physical damages
Mechanical shock (Non operation)		① 294m/s^2 , 11ms ② X, Y, Z directions ③ 3 times each directions	
ESD (Operation)		① 150pF, 150Ω , $\pm 10\text{kV}$ ② 9 places on a panel surface Note3 ③ 10 times each places at 1 sec interval	No display malfunctions
Dust (Operation)		① Sample dust: No.15 (by JIS-Z8901) ② 15 seconds stir ③ 8 times repeat at 1 hour interval Note2	
Low pressure	Non-operation	① 15 kPa (Equivalent to altitude 13,600m) ② $-20^{\circ}\text{C} \pm 3^{\circ}\text{C} \dots 24\text{hours}$ ③ $+60^{\circ}\text{C} \pm 3^{\circ}\text{C} \dots 24\text{hours}$	No display malfunctions
	Operation	① 53.3 kPa (Equivalent to altitude 4,850m) ② $0^{\circ}\text{C} \pm 3^{\circ}\text{C} \dots 24\text{hours}$ ③ $+60^{\circ}\text{C} \pm 3^{\circ}\text{C} \dots 24\text{hours}$ Note2	

Note1: Display and appearance are checked under environmental conditions equivalent to the inspection conditions of defect criteria.

Note2: Luminance: 450cd/m^2 at luminance control.

Note3: See the following figure for discharge points





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7. PRECAUTIONS

7.1 MEANING OF CAUTION SIGNS

The following caution signs have very important meaning. **Be sure to read "7.2 CAUTIONS" and "7.3 ATTENTIONS"!**



This sign has the meaning that a customer will be injured or the product will sustain damage if the customer practices wrong operations.



This sign has the meaning that a customer will be injured if the customer practices wrong operations.

7.2 CAUTIONS



*** Do not shock and press the LCD panel and the backlight! There is a danger of breaking, because they are made of glass. (Shock: Equal to or no greater than 294m/s^2 and equal to or no greater than 11ms, Pressure: Equal to or no greater than 19.6N ($\phi 16\text{mm}$ jig))**

7.3 ATTENTIONS



7.3.1 Handling of the product

- ① Take hold of both ends without touching the circuit board when the product (LCD module) is picked up from inner packing box to avoid broken down or misadjustment, because of stress to mounting parts on the circuit board.
- ② Do not hook nor pull cables such as lamp cable, and so on, in order to avoid any damage.
- ③ When the product is put on the table temporarily, display surface must be placed downward.
- ④ When handling the product, take the measures of electrostatic discharge with such as earth band, ionic shower and so on, because the product may be damaged by electrostatic.
- ⑤ The torque for product mounting screws must never exceed 0.735N·m. Higher torque might result in distortion of the bezel. And the length of product mounting screws must be $\leq 5.0\text{mm}$.

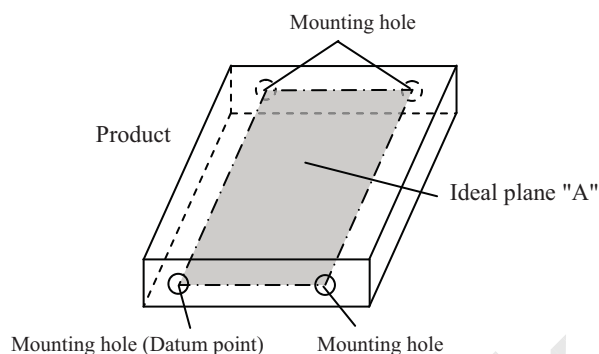
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- ⑥ The product must be installed using mounting holes without undue stress such as bends or twist (See outline drawings). And do not add undue stress to any portion (such as bezel flat area). Bends or twist described above and undue stress to any portion may cause display mura.

Recommended installing method: Ideal plane "A" is defined by one mounting hole (datum point) and other mounting holes. The ideal plane "A" should be the same plane within ± 0.3 mm.



- ⑦ Do not press or rub on the sensitive product surface. When cleaning the product surface, wipe it with a soft dry cloth.
- ⑧ Do not push or pull the interface connectors while the product is working.
- ⑨ When handling the product, use of an original protection sheet on the product surface (polarizer) is recommended for protection of product surface. Adhesive type protection sheet may change color or characteristics of the polarizer.
- ⑩ Usually liquid crystals don't leak through the breakage of glasses because of the surface tension of thin layer and the construction of LCD panel. But, if you contact with liquid crystal by any chance, please wash it away with soap and water.

7.3.2 Environment

- ① Do not operate or store in high temperature, high humidity, dewdrop atmosphere or corrosive gases. Keep the product in packing box with antistatic pouch in room temperature to avoid dusts and sunlight, when storing the product.
- ② In order to prevent dew condensation occurred by temperature difference, the product packing box must be opened after enough time being left under the environment of an unpacking room. Evaluate the storage time sufficiently because dew condensation is affected by the environmental temperature and humidity. (Recommended leaving time: 6 hours or more with the original packing state after a customer receives the package)
- ③ Do not operate in high magnetic field. If not, circuit boards may be broken.
- ④ This product is not designed as radiation hardened.



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7.3.3 Characteristics

The following items are neither defects nor failures.

- ① Response time, luminance and color may be changed by ambient temperature.
- ② Display mura, flickering, vertical streams or tiny spots may be observed depending on display patterns.
- ③ Do not display the fixed pattern for a long time because it may cause image sticking. Use a screen saver, if the fixed pattern is displayed on the screen. 2
- ④ The display color may be changed depending on viewing angle because of the use of condenser sheet in the backlight.
- ⑤ Optical characteristics may be changed depending on input signal timings.

7.3.4 Others

- ① All GND, GNDB, VDD and VDDB terminals should be used without any non-connected lines.
- ② Do not disassemble a product or adjust variable resistors.
- ③ Pack the product with the original shipping package, in order to avoid any damages during transportation, when returning the product to NLT for repairing and so on.
- ④ The LCD module by itself or integrated into end product should be packed and transported with display in the vertical position. Otherwise the display characteristics may be degraded.

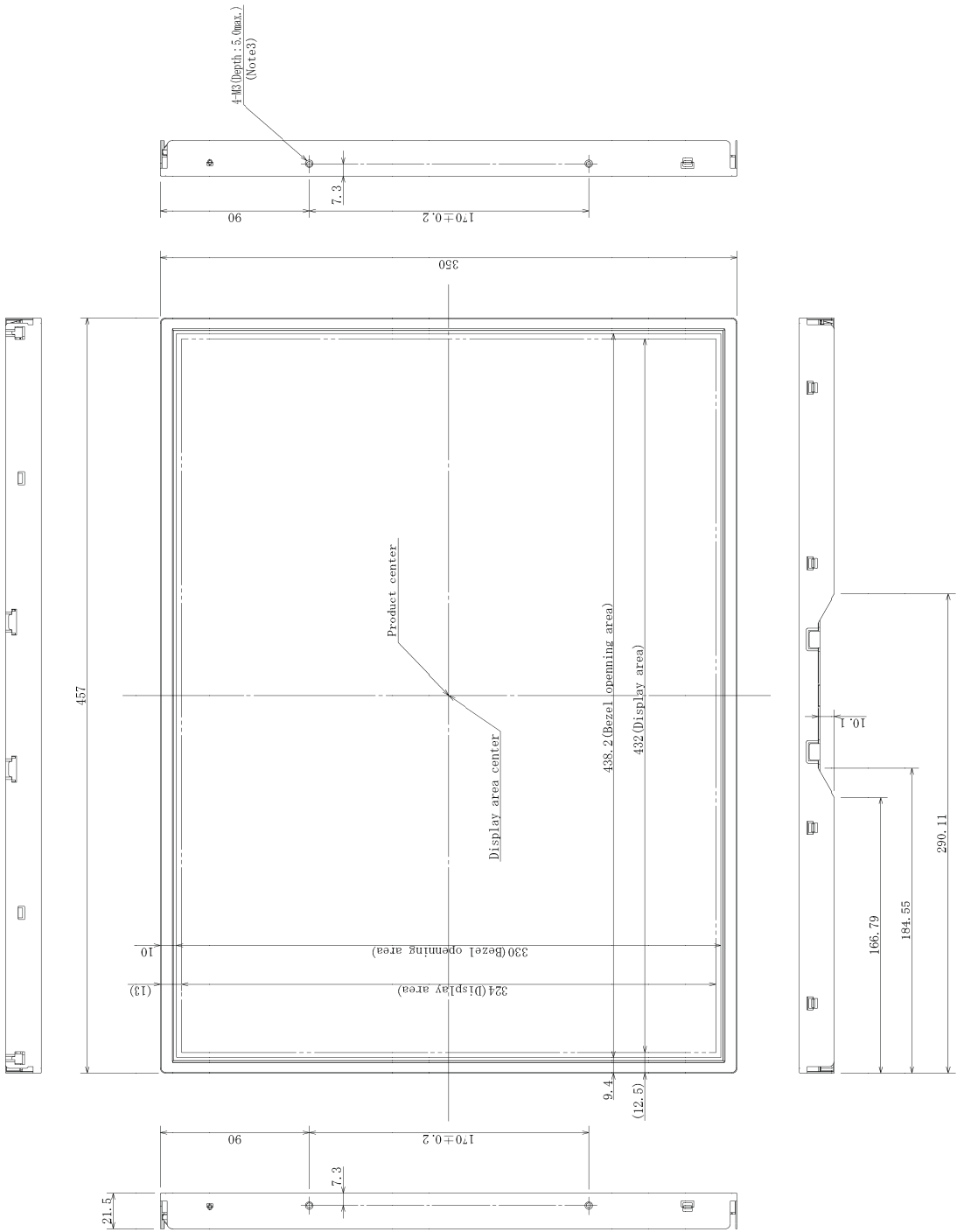


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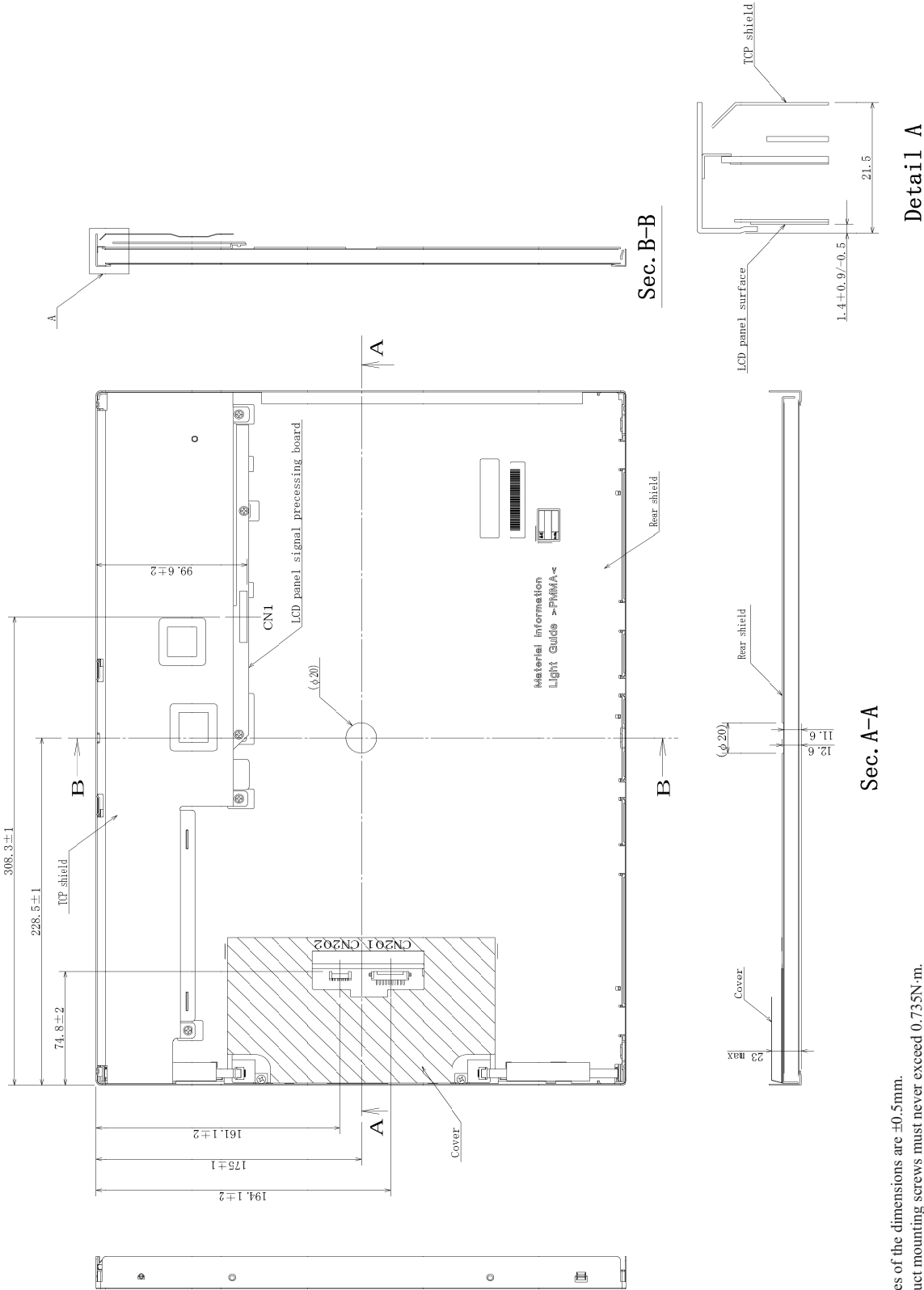
8. OUTLINE DRAWINGS
8.1 FRONT VIEW



- Note1: Not shown tolerances of the dimensions are ±0.5mm.
Note2: The torque for product mounting screws must never exceed 0.735N·m.
Note3: The length of product mounting screws from surface of plate must be ≤ 5.0mm.
Note4: The values in parentheses are for reference.

Unit: mm

8.2 REAR VIEW



Note1: Not shown tolerances of the dimensions are ±0.5mm.
Note2: The torque for product mounting screws must never exceed 0.735N·m.
Note3: The length of product mounting screws from surface of plate must be ≤ 5.0mm.
Note4: The values in parentheses are for reference.

Unit: mm



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REVISION HISTORY

The inside of latest specifications is revised to the clerical error and the major improvement of previous edition. Only a changed part such as functions, characteristic value and so on that may affect a design of customers, are described especially below.

Edition	Document number	Prepared date	Revision contents and signature
1st edition	DOD-PP-1244	July 8, 2011	Revision contents New issue Writer Approved by T. OGAWA Checked by Prepared by T. OGAWA
2nd edition	DOD-PP-1268	Sep 16, 2011	Revision contents P5 General specifications • Luminance: 890 cd/m ² (typ.) → 900 cd/m ² (typ.) • Signal system: THC63LVD824 → THC63LVD824A • Power consumption: (52) W (typ.) → (57) W (typ.) P7 Mechanical specifications • Module size: TBD (max. D) mm → 23.0 (max. D) mm • Weight: TBD (max.) g → (2,980) (max.) g P7 Absolute maximum ratings • Power supply voltage- LED driver board: -0.3 to +27.0 V → -0.3 to +15.0 V • Operating temperature- Rear surface: (0 to + TBD) °C → (0 to + 60) °C P8 LCD panel signal processing board • Power supply current: TBD (max.) mA → (700) (max.) mA P9 LED Driver board • Power supply current: (5,000) (typ.) mA → (4,200) (typ.) mA P9 LED Driver board current wave • (5,000) mA (typ.) → (4,200) mA (typ.) • At the minimum luminance control: TBD % → (1) % (At frequency: 325 Hz) P10 Power supply voltage ripple (addition), Fuse (addition) P11 LED Driver board • tr ≤ TBD ms → tr ≤ (100) ms • Note2: TBD → (100) ms P15 Luminance control methods • Variable resistor control- Luminance ratio: 0Ω: TBD % → 0 % • Voltage control- Luminance ratio: 0V: TBD % → 0 % • Pulse width modulation- Luminance ratio : TBD, TBD % → (0.01), (1) %, (At frequency: 325 Hz) • Note4: "4.6.3 Detail of BRTP timing" → "4.6.2 Detail of BRTP timing" P16 Detail of BRTP timing- Each parameter • Luminance control frequency: (325) (max.) Hz → (1,000) (max.) Hz • Parameter: Duty ratio → External PWM pulse width P17 LVDS data input map- Mode A • Transmitter: THC63LVDF83A → THC63LVDM83D, THC63LVD823 → THC63LVD823B P24-25 Optical characteristics • Luminance: 890 cd/m ² (typ.) → 900 cd/m ² (typ.) • Color uniformity (addition) • Response time: Ton / Toff: TBD (max.) ms → (30) (max.) ms • Viewing angle- Measuring instrument: BM-5A (addition) • Note3: TopF = TBD°C → TopF = 32°C • Note4: TopF = TBD°C → TopF = 30°C Temperature difference in display area: ΔTBD°C (addition) • Note7 (addition) • Definition of color uniformity (addition)



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REVISION HISTORY

Edition	Document number	Prepared date	Revision contents and signature									
2nd edition	DOD-PP-1268	Sep 16, 2011	Revision contents P30 Characteristics • Optical characteristics ..., because the LCD has cold cathode fluorescent lamps. (elimination) P31-32 Outline drawings- Front view • Front view • 7.5 → 7.3 (2 points), 8.9 → 10.1 • Display center → Product center • 92, 122.3 (elimination) • 166.79, 184.55, 290.11 (additon) • Rear view • Cover: figure is changed. Signature of writer <table><tr><td>Approved by</td><td>Checked by</td><td>Prepared by</td></tr><tr><td></td><td></td><td></td></tr><tr><td>T. OGAWA</td><td></td><td>T. OGAWA</td></tr></table>	Approved by	Checked by	Prepared by				T. OGAWA		T. OGAWA
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